**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-14 (canceled)

15. (new) A method for fast clock timing recovery from transmitted data between a master XDSL modem and a slave XDSL modem wherein said data is submitted over an XDSL transmission medium comprising the steps of:

(a) Providing the master modem, synchronized by its own timing clock, for data transmission,

(b) Providing the slave modem, synchronized by its own timing clock, for data reception,

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(c) Providing the transmission medium connecting the master and the slave modems,

(d) Encoding and transmitting the data at the mater modem as a sequence of symbols using pre-determined QAM states, said sequence having a frequency,

(e) Receiving the data at the slave modem as a sequence of symbols,

(f) Sampling the received data at a symbol rate and converting the sampled data into digital form,

(g) Splitting the digitally converted data into in-phase (I) and quadrature (Q) channels,

(h) Low-pass filtering of the data corresponding to the in-phase and quadrature channels,

(i1) Re-sampling the filtered data at a re-sampling rate which is at least twice the symbol rate,

(i2) Modulating each re-sampled data with the two discrete-time sequences:

$\cos(0.5\,\pi\,n) = \ldots, 1, 0, -1, 0, \ldots$

$\sin(0.5\,\pi\,n) = \ldots, 0, 1, 0, -1, \ldots$

(i3) Computing a normalized spectral line vector corresponding to the re-sampled modulated data,

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(i4) Tuning the symbol rate in dependence of the imaginary part of the normalized line vector for tracking the frequency of the incoming symbols.

16. (new) The method according to claim 15 wherein the step h) of low-pass filtering comprises filtering each channel with digital low-pass filters, said filters being matched to transmitting filters at the master modem; and the steps i1) to i4) comprise turning the clock timing recovery into a blind mode, by the steps of:

(a) Re-sampling the filtered I and Q data at twice the symbol rate;

(b) Extracting lower and upper band edge components by modulating each of the sampled sequence of I and Q data of step (1) above with the said two discrete time sequences;

(c) Filtering the four resulting products with four first order low-pass filters and re-sampling the results at the symbol rate;

(d) Computing real imaginary parts of the corresponding spectral line vector using the products of step (3) above;

(e) Filtering both the real and the imaginary parts of step (4) above, using another first order low-pass filter;

(f) Normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(g) Extracting the phase of the spectral line vector from the normalized imaginary part of step (6) above;

(h) Feeding the imaginary part of step (7) above as a phase-error signal to a controller of a phase-locked loop (PLL), said controller outputting a digital control signal, said PLL utilizing a frequency controlled clock tracking oscillator, the frequency of which is tuned to track the frequency of the received sequence of symbols (the master modem clock frequency);

(i) Converting the digital control signal to an analog control voltage supplied to the clock tracking oscillator of step (8) above, using a Digital to Analog Converter (DAC); and

(j) Using a secondary accumulator to correct the control word supplied to the DAC of step (9) above.

17. (new) The method according to claim 16 wherein the method further comprises the steps:

(a) Feeding the filtered I and Q data to a complex linear equalizer for coarse phase and amplitude error correction;

(b) Computing symbol state data decisions and outputting said decisions using a slicer circuitry;

(c) Fine equalization of channel distortions by feeding the I and Q outputs of the slicer to a decision feedback equalizer, the outputs of which are extracted from the slicer I and Q inputs, respectively;

(d) Computing an extracted symbols error rate at the slicer outputs; and

(e) After an error probability decreases to a given BER, switching from blind mode timing recovery to a data directed timing recovery mode.

18. (new) The method according to claim 15 wherein the transmission medium is a pair of copper wires.

19. (new) The method according to claim 15 wherein the pair of copper wires is a telephone line.

20. (new) The method according to claims 16 wherein the tracking oscillator utilized by the phase-locked loop is a Voltage-Controlled Crystal Oscillator (VCXO).

21. (new) The method according to claim 16 wherein the blind timing recovery is achieved using a reduced constellation.

22. (new) The method according to claim 21 wherein the reduced constellation comprises only equal amplitude symbols.

23. (new) The method according to claim 16 wherein the blind timing recovery is achieved using full constellation.

24. (new) The method according to claim 16 wherein the digital control signal of the PLL tracking oscillator is provided accurately in double precision and converted using an up to 8 bit Digital to Analog Converter (DAC) means, the method further comprising the steps of:

(a) Rounding the double precision control signal;

(b) Generating an error signal between the double precision value and the rounded value;

(c) Accumulating the error signal in a secondary accumulator;

(d) Adding the error signal to the output signal of the secondary accumulator;

(e) Comparing the result of step d) above with half the value of the DAC's LSB;

(f) Compensating the rounded value according the result of step e) above by the steps of:

(g) Adding the value of the DAC's LSB to the accumulator output, if the output value is larger than half the value of the DAC's LSB; or

(h) Subtracting the value of the DAC's LSB from the accumulator output, if the output value is smaller than half the value of the DAC's LSB.

25. (new) An XDSL modem for fast clock timing recovery from a received data signal, said data signal transmitted by a master XDSL modem and transferred over an XDLS-transmission medium, comprising:

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(a) An input for receiving the transmitted data signal comprising a sequence of symbols, said sequence having a frequency;

(b) A first Analog to Digital Converter connected to the input for sampling and digitizing the received signal at a symbol rate;

(c) Two first multipliers connected to the first Analog to Digital Converter for splitting the sampled data signal into in-phase (I) and quadrature (Q) channels, said first multipliers being phase-shifted by 90°;

(d) Two first digital low-pass filters for filtering each channel, said filters being connected to the first multipliers and being matched to transmitting filters at the master modem;

(e) A clock timing recovery circuit operating in blind mode, comprising:

(1) Means for sampling the filtered I and Q channels at twice the symbol rate;

(2) Four second multipliers connected to the means for sampling for modulating each of the sampled sequence of I and Q channels with two discrete time sequences:

$\cos(0.5\,\pi\,n) = \ldots, 1, 0, -1, 0, \ldots$

$\sin(0.5\,\pi\,n) = \ldots, 0, 1, 0, -1, \ldots$

for extracting lower and upper band edge components;

(3) Four second first order low-pass filters connected to the second multipliers for filtering the four resulting products of the four second multipliers and for resampling the results at the symbol rate;

(4) A spectral line computer connected to the four second first order low-pass filters for computing real and imaginary parts of a spectral line vector;

(5) At least one third first order low-pass filter connected to the spectral line computer for filtering both the real and the imaginary parts of the spectral line vector;

(6) A spectral line normalizer connected to the third first order low-pass filters for normalizing the magnitude of the spectral line vector to unity using a suitable automatic gain control circuitry;

(7) A Controller connected to the spectral line normalizer, the controller being part of a phase-locked loop (PLL) and said controller outputting a digital control signal, said PLL utilizing a frequency controlled clock tracking oscillator, the frequency of which is tuned to track the frequency of the received sequence of symbols (the master modem clock frequency);

(8) A second Digital to Analog Converter (DAC) connected to the controller for converting the digital control signal to an analog control voltage supplied to the tracking oscillator of the PLL:

(f) A complex linear equalizer connected to the two first multipliers for coarse phase and amplitude error correction;

(g) A slicer circuitry connected to the complex linear equalizer for computing and outputting I and Q symbol state date decisions;

(h) A decision feedback equalizer connected to the outputs of the slicer circuitry and connected via an adder to the slicer circuitry input for fine equalizing channel distortions;

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(i) Circuitry connected to the outputs of the slicer circuitry for computing an extracted symbols error rate; and

(j) Circuitry for switching from blind timing recovery mode to data directed timing recovery mode, once the error is reduced to less than a given BER.

26. (new) The modem according to claim 25 wherein the modem further comprises:

(9) A circuitry for accumulation to correct the digital control signal supplied to the second DAC, said digital control signal having double precision accuracy, comprising:

(a) Circuitry for rounding the double precision digital control signal;

(b) Circuitry for generation of an error signal between the double precision value and the rounded value;

(c) Circuitry for accumulation of the error signal in a secondary accumulator;

(d) A first adder for adding the error signal to the output signal of the secondary accumulator;

(e) A comparator for comparing the output of the adder with half the value of the second DAC's LSB;

(f) A second adder for compensating the rounded value according to the result of the comparator by

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(i1) Adding the value of the second DAC's LSB to the accumulator output, if the output value is larger than half the value of the second DAC's LSB, and

(i2) Subtracting the value of the second DAC's LSB from the accumulator output, if the output value is smaller than half the value of the second DAC's LSB.

**Amendments to the Drawings:**

The attached sheets of drawings include Figures 1-3. In Figures 1-3, previously omitted legend "Prior Art" has been added.

Attachment: Replacement Sheets